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Development of an Analytical Model of Drain Current for Junctionless GAA MOSFET including Source/Drain Resistance

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*Abstract*—Fabrication of devices in deca-nanometer regime suffers from several limitations as the devices are being scaled in order to increase the speed and transistor density. This has led to a series of innovative techniques by the industry as well as academia. Formation of depletion regions associated with the p-n junctions in junction based (JB) metal-oxide-semiconductor field-effect transistors (MOSFETs) is one of the restrictive factors in scaling short channel devices. This has led to several short channel effects (SCEs). Recently, novel MOSFET structures devoid of p-n junctions have been developed and fabricated successfully. Such devices are named “junctionless transistors (JLTs)”. MOSFETs utilizing gate-all-around (GAA) architecture has been reported to be the ultimate device structures in silicon integrated circuits (ICs). In this paper, we have, therefore, developed an analytical short channel drain current model for GAA JLT, including source (S)/drain (D) series resistance, which is also one of the important parameters when devices with short channel are fabricated. We have obtained the potential distribution profile using Poisson’s equation, which was then used to obtain the drain current model. The model has been validated with both the experimental as well as simulation results. We have further analyzed the effect of S/D resistance on the drain current for different device parameters.

*Index Terms*— GAA, Junctionless. Short channel

# Introduction

Limitations of the present-day fabrication techniques in the nanometer regime have led to the innovation of alternative device structures, to keep in line with the Moore’s law. One of the challenging factors that needs to be overcome in short channel (SC) junction based (JB) metal-oxide-semiconductor field-effect transistors (MOSFETs) is the fabrication of sharp and abrupt junctions between the channel and source/drain (S/D) region. A lot of short channel effects (SCEs) are associated with the formation of these junctions. Such challenges led to the development of Junctionless (JL) structures in which the concentration of dopants is uniform all over the S/D region and the channel region (Colinge et al. 2010). As a result, there is no longer a need for expensive ultra-fast annealing techniques, which lessen the demands on fabrication processes and the thermal budget (Colinge 2007; Colinge et al. 2010). This permits one to fabricate SC devices. Simple architecture (no p-n junction), no concentration gradient, low leakage and improved short channel characteristics are some of the advantages of JLTs. ers in adopting blockchain technologyractsby any of the agencyywhere else or submitted er based scaffolding. nce).h respect to

Compared to other multi-gate structures, MOSFETs with GAA structure provides better immunity to SCEs, as the gate effectively controls the electrostatic potential inside the channel. Incorporating GAA in JL devices can further enhance the device characteristics (Colinge et al. 2010; Duarte et al. 2011; Yu 2014). The current research therefore focusses on the GAA JLTs.

There are numerous reports on drain current modeling of long channel GAA JLT (Duarte et al. 2011; Yu 2014). However, a few have reported the modeling of short channel devices (Hu et al. 2014; Jiang et al. 2014; Raut & Nanda 2022; Smaani et al. 2022). In this paper, we have developed an analytical short channel drain current model of GAA JLT, which is a recent area of research (Chaujar et al. 2023; Kumar et al. 2023; Kumari et al. 2023; Smaani et al. 2024), based on the previous compact model of junction-based GAA MOSFETs (Tsormpatzoglou et al. 2009), incorporating S/D series resistance. The S/D series resistance plays an important role in modeling of SC devices as in such devices, the series resistance becomes a considerable portion of the total resistance and hence needs to be considered in the device modeling. The model has been validated with both the experimental as well as simulation data. The effect of change in series resistance on the drain current characteristics has also been obtained.

# Theoretical Details

GAA structures offer superior short-channel characteristics due to the excellent control of gate over the channel in such structures. Due to the absence of junctions in JLTs, there is no requirement of doping concentration gradient and hence the problems associated with junctions are eliminated. The device is also reported to deliver improved driving current and sub-threshold properties when combined with GAA architecture. Figure 1 depicts the cross-section of such JL GAA MOSFET.

## Device Physics

The JLT can be characterized as a device that is strongly and evenly doped throughout. This means the type of the dopant and its concentration is same all over the junction. The gate materials used are p+ polysilicon for n-type devices and n+ polysilicon for p-type devices. Thus, there is a work function difference of approximately 1eV resulting in the depletion of

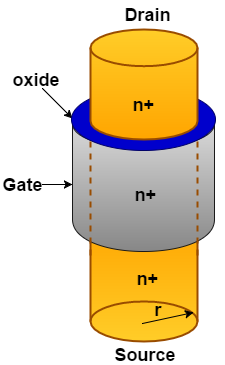


Figure 1. Cross section of cylindrical Gate All Around MOSFET.

the channel. Gate bias must be applied to bring the channel out of depletion. The working principle of GAA JLT is as follows.

In the absence of gate voltage (*Vg*), the channel is fully depleted and between the source and the drain regions, a negligible amount of current flows. In such a situation, the transistor is said to be in the sub-threshold region of operation or in OFF condition. The valence band is completely filled while the conduction band is empty. Now if a gate voltage equal to the threshold voltage (*VTH*) of the device is applied, a thin neutral path (non-depleted region) is formed at the center of the channel over which bulk current flows. Increasing the gate voltage widens the path which increases the current flowing through it. This has been reflected in the energy band diagram where the concentration of positive charges in the valence band is reduced. A complete neutral channel is created when the applied *VG* becomes equal to the flat-band voltage (*VFB*). The device is now said to be in the flat-band condition as the conduction and valence bands become flat. It is now said to be turned ON. On further increasing the gate voltage accumulation layer is created at the surface and the negative charge carriers get accumulated at the surface resulting in the flow of surface current along with the bulk current. The schematic representation of GAA JLT in different regions of operation along with their corresponding energy-band diagram is shown in Figure 2.

The Poisson’s equation in the cylindrical coordinate for n-type semiconductor can be expressed as

 (1)

where, *ϕ* represents the potential,

*r* represents the radial direction,

*V* is the applied voltage,

*VT* is thermal voltage,

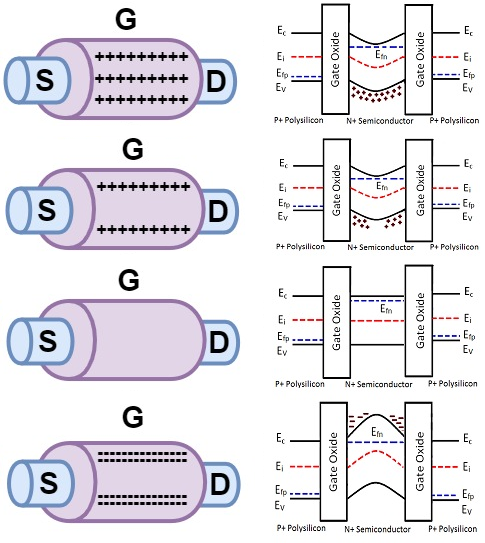


Figure 2. GAA JLT in different regions of operation.

*εSi* is the permittivity of Si, and

*Nd* is the uniform doping concentration throughout the source, drain and channel.

Considering only mobile carrier’s density and neglecting depletion charge density, the above equation can be simplified (Trevisoli et al. 2012) as

 (2)

Boundary conditions applied for the GAA MOSFET can be expressed as (Jimenez et al. 2004)

 (3)

The change in threshold voltage Δ*VTH*, due to short channel can be expressed as (Tsormpatzoglou et al. 2009)

 (4)

where *VTH*,*L* and *VTH*,*S*are the long channel (Duarte et al. 2011) and short channel (Chiang 2012) threshold voltages of GAA JLT respectively.

Considering the drift-diffusion model, the drain current can be expressed as

 (5)

In the above equation, *qi* = *Qi*(*V*)/(4*εsikT*/*qtsi*), represents the normalized sheet charge density, *Qi* is the inversion charge density, and *V* varies from source to drain voltage.

On integrating the above equation, the drain current expression is obtained as

 (6)

The expression for mobility can be represented as (Gaubert et al. 2010)

 (7)

where, *α*, *θ1* and *θ2* accounts for the Coulomb scattering, phonon scattering and scattering due to surface roughness respectively. *Vgs* is the gate to source voltage, *µ0* is the low field mobility. Further, we have also considered the effect of channel length modulation by a factor FCLM (Tsormpatzoglou et al. 2009), which is expressed as

 (8)

where

 (9)

 (10)

 (11)

 (12)

λ represents the distance by which the drain electric field penetrates into the channel. Replacing *µ* by *µeff* and multiplying FCLM to equation (6), the final drain current expression is given by

 (13)

In short channel devices, the series resistance (*Rsd*) constitutes a large portion of the total resistance due to the reduction in intrinsic channel resistance. The series resistance reduces the supply voltages and degrades device driving capability. The extracted *Rsd* has been incorporated via following equations

 (14)

 (15)

The intrinsic gate and drain voltages are represented by *V’gs* and *V’ds* respectively. On incorporation of series resistance, the gate and drain voltages in the above mentioned equations (7-

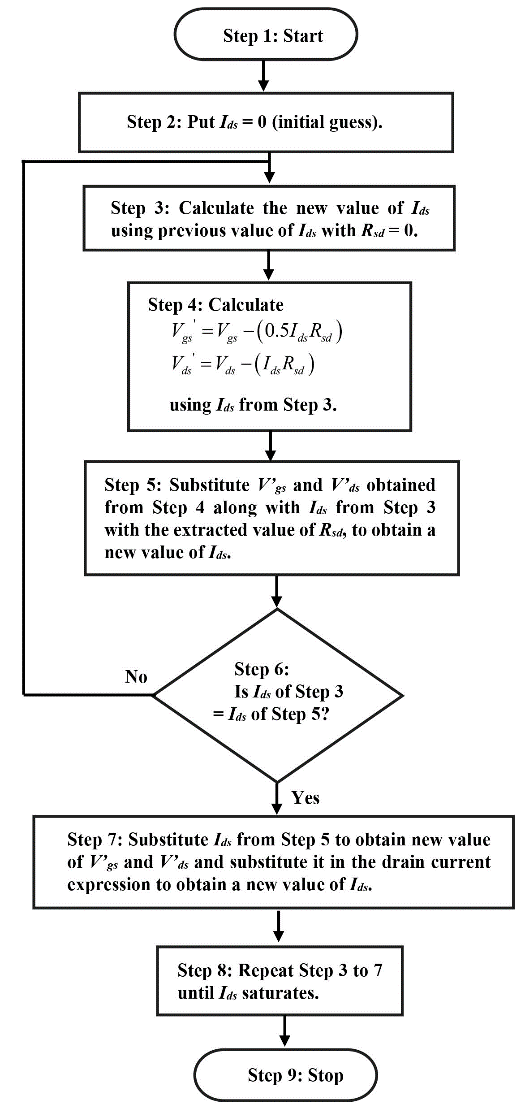


Figure 3. Flowchart showing the calculation of *Ids*.

13) are replaced by the intrinsic voltages. On incorporating the above equations in the expressions of mobility and drain current, new expression of drain current is obtained.

From above equations, it is observed that the supply voltages are the functions of drain current. Thus, an iterative procedure has been utilized to calculate the supply voltages as well as the drain current (Kumar et al. 2016; 2017).

The iterative process used is depicted in Figure 3 in the form of a flowchart. The steps taken are: Initially the drain current is taken as zero. Then, in 1st iteration *Ids* is calculated using equation (13) with *V’gs* and *V’ds* obtained from (14) and (15) respectively (with *Ids* = 0 initially). Now, using the value of *Ids* obtained from the previous step, voltages *V’gs* and *V’ds* are calculated (using (14) and (15)). Now, in second iteration, *Ids* is obtained by substituting the calculated values of *V’gs* and *V’ds* along with the value of *Ids* obtained from the previous step. This procedure is repeated until consecutive constant values of *Ids* are obtained.

# Validation Of The Model

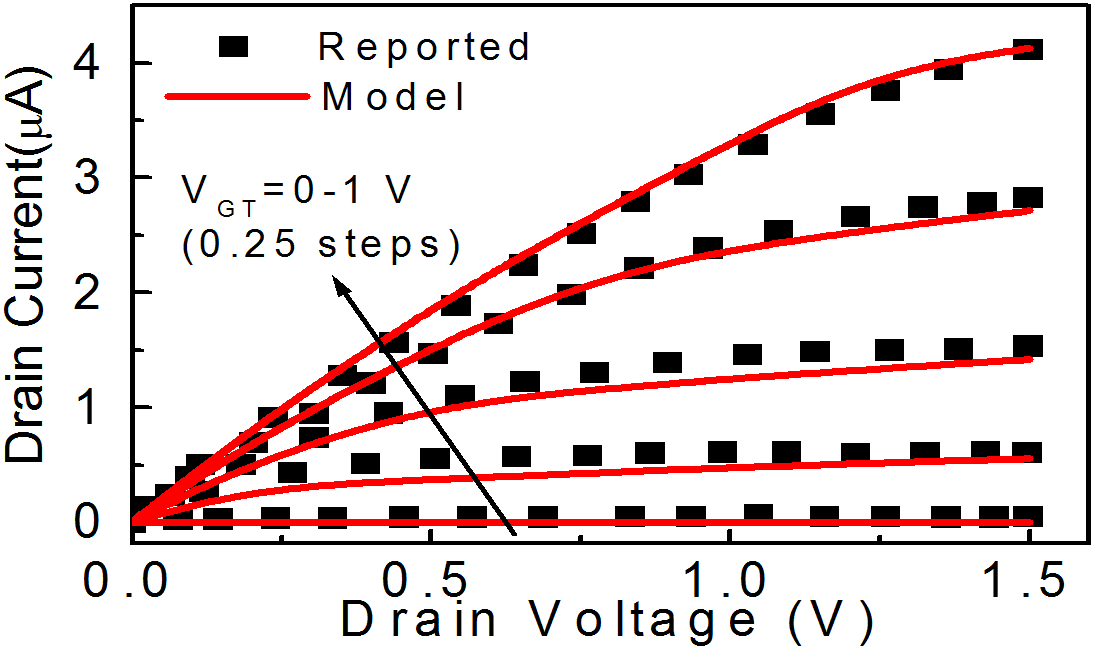
The drain current model has been validated with both the experimental and the simulation data. The model has been verified with devices having different channel lengths ranging from 20 nm to 160 nm. The range of parameters *Vsc* and *Qsc* have been taken as 0.2-1.3 in all our computations. Figure 4 (a) and (b) shows the validation with experimental data (Singh et al. 2011) and (Moon et al. 2013).

In order to validate the accuracy of the model with the experimental data, the effect of source-drain series resistance (*Rsd*) has been incorporated. The source-drain series resistances were extracted (Kim et al. 2013) and were used in the calculations. From the figure, it is observed that the model agrees well with the experimental records.

Figure 5 illustrates the verification of the model with another experimental data (Choi et al. 2011). Here the gate length, effective oxide thickness (EOT) and doping concentration are 50 nm, 13 nm and 2×1019 cm-3 respectively.



**(a)**



**(b)**

Figure 4. Validation of the model with the reported data (a) (Singh et al. 2011); (b) (Moon et al. 2013). (Parameters Used: (a) *L*= 160 nm; *ND* = 6.7 ×1018 cm-3; (b) *L* = 150 nm; Width of NW =18 nm).

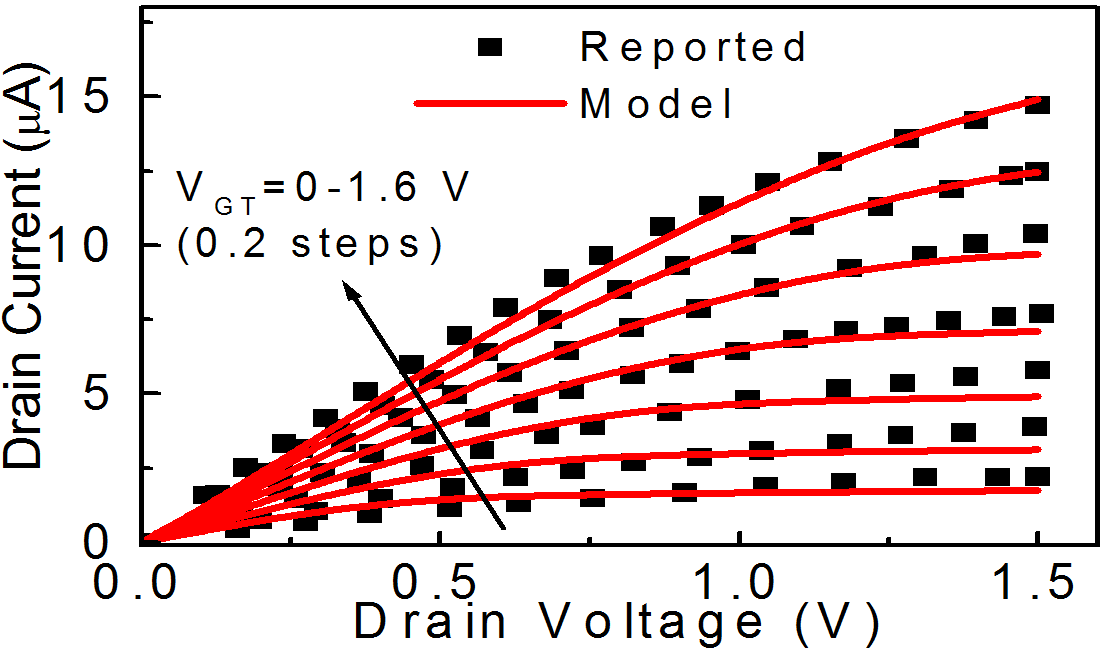
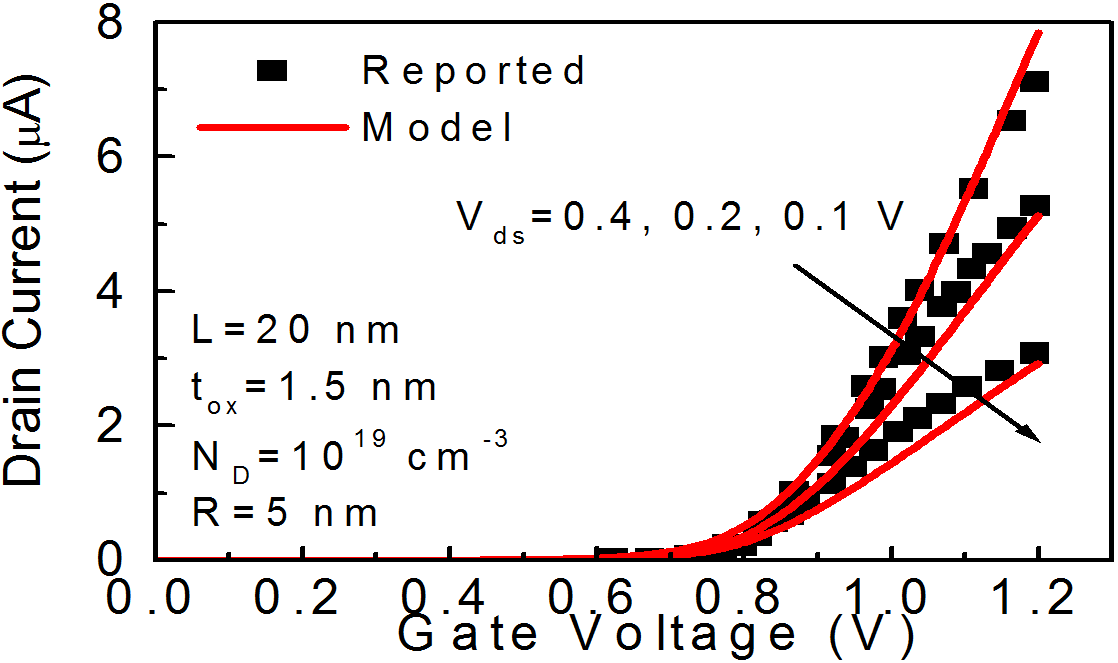


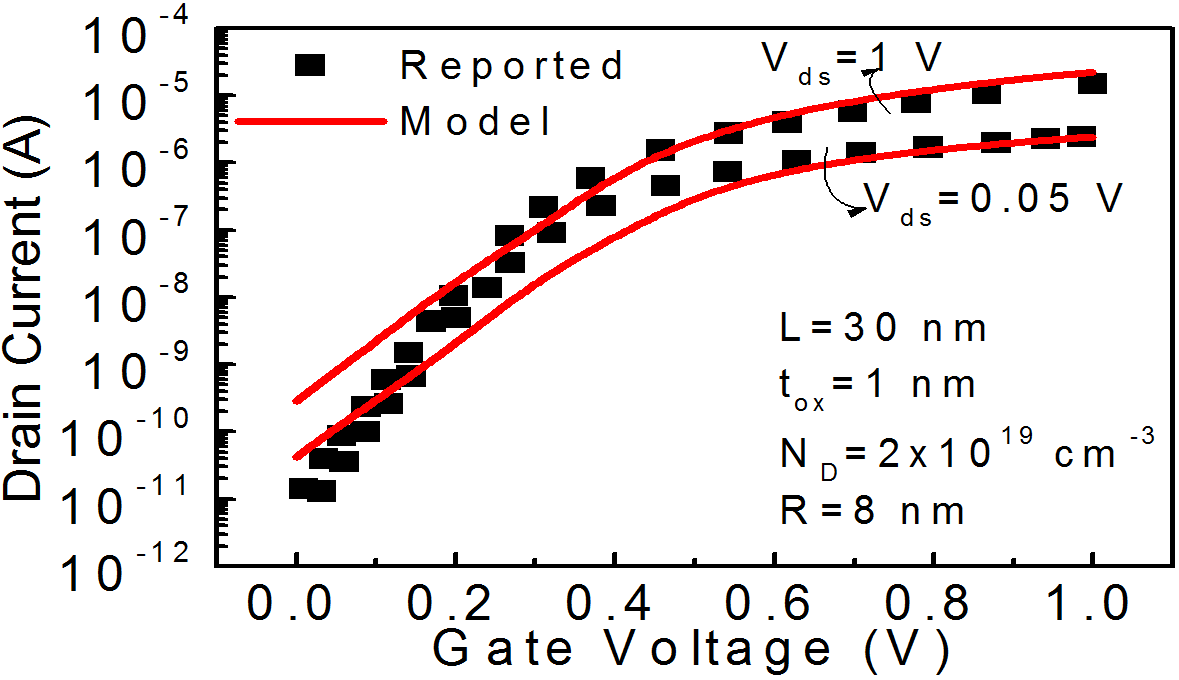
Figure 5. Validation of the model with the experimental data (Choi et al. 2011). (Parameters Used: *L* = 50 nm, EOT=13 nm and *ND* = 2×1019 cm-3)

Using the extracted value of *Rsd* = 15 KΩ, the drain current has been computed using the model. The results obtained are in line with the experimental values with deviation from the reported one below 5%.

The model has also been compared with the simulation data. The drain current characteristics of GAA JLT with channel length 20 nm and 30 nm are presented in Figure 6 (a) and (b) respectively, for different drain voltages. As depicted from the figure, the model shows good accuracy with the reported



**(a)**



**(b)**

Figure 6. Validation of the model with the reported data (a) Hu et al. 2014); (b) (Wang et al. 2014).

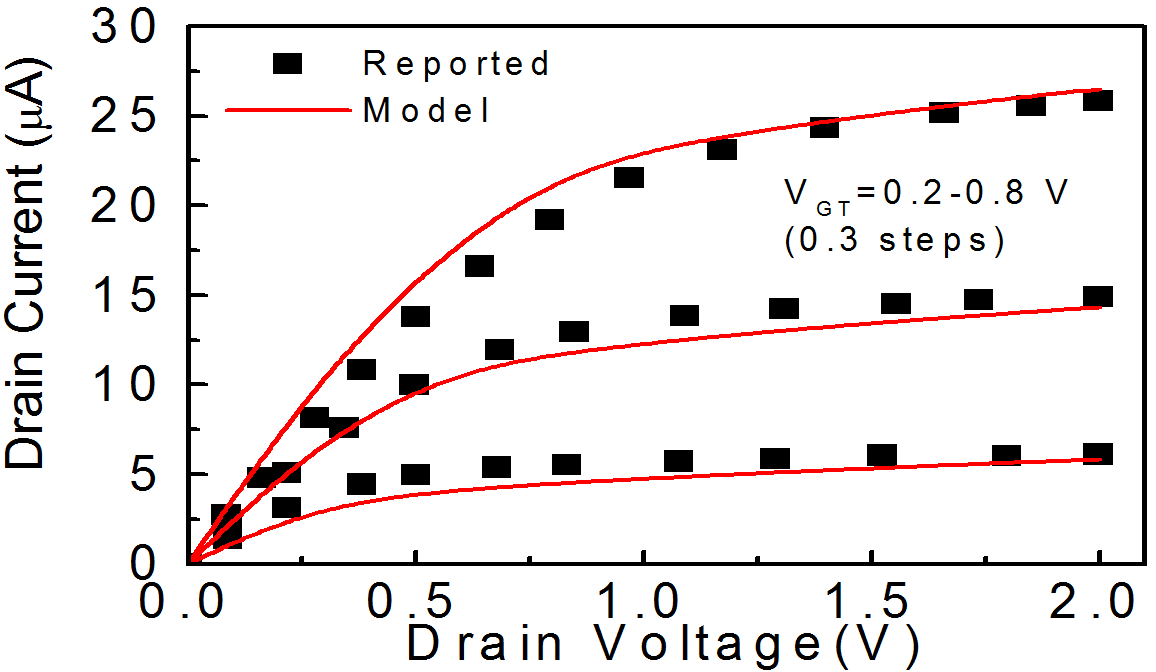


Figure 7. Comparison of simulated (Lou et al. 2012) and modeled output characteristics with *L* = 40 nm, *tox* = 2 nm, *R* = 5 nm and *ND* = 2×1019 cm-3.

simulation data (Hu et al. 2014; Wang et al. 2014).

We have validated the model with another simulated data (Lou et al. 2012), shown in Figure 7. The channel length, oxide thickness and doping concentration are 40 nm, 2 nm and 2×1019 cm-3 respectively. A good agreement is obtained between the results from the model and simulation, that further supports the accuracy of the model.

# Results and Discussion

Figure 8 depicts the change in drain current with and without incorporating *Rsd* for different drain voltages. From the figure, it can be obtained that the drain current decreases with inclusion of *Rsd*, due to the reduction in terminal voltages.

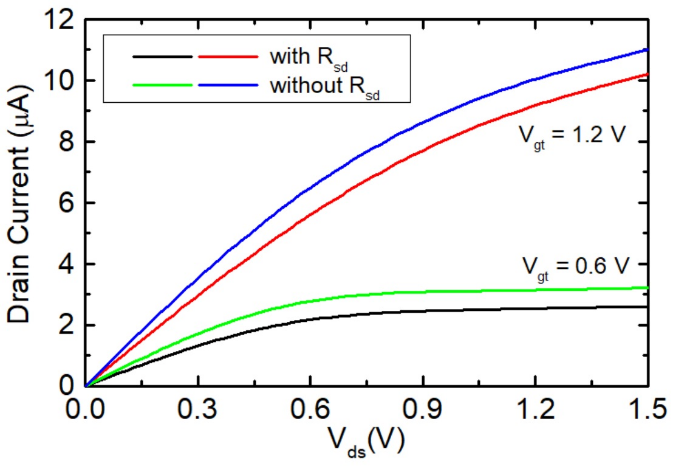


Figure 8. Variation of the drain current with different drain voltages with and without S/D resistance (Parameters Used: *L* = 50 nm, EOT = 13 nm and *ND* = 2×1019 cm-3, *Rsd* = 15 kΩ).

The variation in the drain current with changes in the gate overdrive voltage (*Vgt* = *Vgs* – *VTH*) for different S/D resistance has also been plotted and depicted in Figure 9.

# Conclusion

To summarize, we have proposed a model of drain current for short channel JL GAA NW n- MOSFET incorporating S/D series resistance. The proposed model has been validated with experimental and simulation data. We have also presented algorithm based on multi-iterative technique for the computation of the drain current. These iterations are necessary

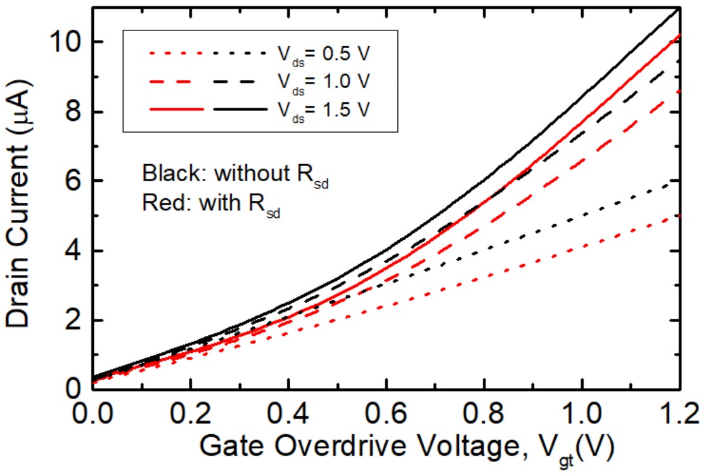


Figure 9. Variation of the drain current with gate overdrive voltage with and without S/D resistance (Parameters Used: *L* = 50 nm, EOT = 13 nm and *ND* = 2×1019 cm-3, *Rsd* = 15 kΩ).

because upon including S/D series resistance, the drain current transforms into the transcendental equation, resulting in a number of coupled equations involving the mobility, threshold voltage, and other variables. The effect of *Rsd* on the drain current has also been investigated. The proposed model may be helpful to the research community in predicting the performance parameters of the devices and circuits before going into final fabrication. This may save time as well as re-sources. We have not taken quantum mechanical effects into account which becomes significant in ultra scaled devices.

# References

Chaujar, Rishu, and Mekonnen Getnet Yirak. 2023. "Sensitivity Investigation of Junctionless Gate-all-around Silicon Nanowire Field-Effect Transistor-Based Hydrogen Gas Sensor." *Silicon* 15(1): 609-621.

Chiang, Te-Kuang. 2012. "A new quasi-2-D threshold voltage model for short-channel junctionless cylindrical surrounding gate (JLCSG) MOSFETs." *IEEE Transactions on Electron Devices* 59 (11): 3127-3129.

Choi, Sung-Jin, Dong-Il Moon, Sungho Kim, Jae-Hyuk Ahn, Jin-Seong Lee, Jee-Yeon Kim, and Yang-Kyu Choi. 2011. "Nonvolatile memory by all-around-gate junctionless transistor composed of silicon nanowire on bulk substrate." *IEEE Electron Device Letters* 32 (5): 602-604.

Colinge, Jean Pierre. 2007. "Multi-gate SOI MOSFETs." *Microelectronic Engineering* 84 (9-10): 2071-2076.

Colinge, Jean-Pierre, Chi-Woo Lee, Aryan Afzalian, Nima Dehdashti Akhavan, Ran Yan, Isabelle Ferain, Pedram Razavi et al. 2010. "Nanowire transistors without junctions." *Nature Nanotechnology* 5 (3): 225-229.

Duarte, Juan P., Sung-Jin Choi, Dong-Il Moon, and Yang-Kyu Choi. 2011. "A nonpiecewise model for long-channel junctionless cylindrical nanowire FETs." *IEEE Electron Device Letters* 33 (2): 155-157.

Gaubert, Philippe, Akinobu Teramoto, and Tadahiro Ohmi. 2010. "Modelling of the hole mobility in p-channel MOS transistors fabricated on (1 1 0) oriented silicon wafers." *Solid-State Electronics* 54 (4): 420-426.

Hu, Guangxi, Ping Xiang, Zhihao Ding, Ran Liu, Lingli Wang, and Ting-Ao Tang. 2014. "Analytical models for electric potential, threshold voltage, and subthreshold swing of junctionless surrounding-gate transistors." *IEEE Transactions on Electron Devices* 61 (3): 688-695.

Jiang, Chunsheng, Renrong Liang, Jing Wang, and Jun Xu. 2014. "Analytical short-channel behavior models of Junctionless Cylindrical Surrounding-Gate MOSFETs." In 2014 *International Symposium on Next-Generation Electronics* (*ISNE*), 1-2. IEEE.

Jimenez, David, Benjamn Iniguez, Jordi Sune, Lluis F. Marsal, Josep Pallares, Jaume Roig, and David Flores. 2004. "Continuous analytic IV model for surrounding-gate MOSFETs." *IEEE Electron Device Letters* 25 (8): 571-573.

Kim, Ye-Ram, Sang-Hyun Lee, Chang-Woo Sohn, Do-Young Choi, Hyun-Chul Sagong, Sungho Kim, Eui-Young Jeong et al. 2013. "Simple S/D series resistance extraction method optimized for nanowire FETs." *IEEE Electron Device Letters* 34 (7): 828-830.

Kumar, Alok, Tarun Kumar Gupta, Bhavana P. Shrivastava, and Abhinav Gupta. 2023. "Impact of temperature variation on noise parameters and HCI degradation of Recessed Source/Drain Junctionless Gate All Around MOSFETs." *Microelectronics Journal* 134: 105720.

Kumar, Subindu, Amrita Kumari, and Mukul Kumar Das. 2016. "Development of a simulator for analyzing some performance parameters of nanoscale strained silicon MOSFET-based CMOS inverters." *Microelectronics Journal* 55: 8-18.

Kumar, Subindu, Amrita Kumari, and Mukul Kumar Das. 2017. "Modeling gate-all-around Si/SiGe MOSFETs and circuits for digital applications." *Journal of Computational Electronics* 16: 47-60.

Kumari, Amrita, Ashish Saini, Amit Kumar, Vivek Kumar, and Mukesh Kumar. 2023. "Recent Developments and Challenges in Strained Junctionless MOSFETs: A Review." In 2023 *International Conference on Computational Intelligence and Sustainable Engineering Solutions (CISES)*, pp. 118-122. IEEE.

Lou, Haijun, Lining Zhang, Yunxi Zhu, Xinnan Lin, Shengqi Yang, Jin He, and Mansun Chan. 2012. "A junctionless nanowire transistor with a dual-material gate." *IEEE Transactions on Electron Devices* 59 (7): 1829-1836.

Moon, Dong-Il, Sung-Jin Choi, Juan Pablo Duarte, and Yang-Kyu Choi. 2013. "Investigation of silicon nanowire gate-all-around junctionless transistors built on a bulk substrate." *IEEE Transactions on Electron Devices* 60 (4): 1355-1360.

Raut, Pratikhya, and Umakanta Nanda. 2022. "A charge-based analytical model for gate all around junction-less field effect transistor including interface traps*." ECS Journal of Solid State Science and Technology* 11 (5): 051006.

Singh, Pushpapraj, Navab Singh, Jianmin Miao, Woo-Tae Park, and Dim-Lee Kwong. 2011. "Gate-all-around junctionless nanowire MOSFET with improved low-frequency noise behavior." *IEEE Electron Device Letters* 32 (12): 1752-1754.

Smaani, Billel, Shiromani Balmukund Rahi, and Samir Labiod. 2022. "Analytical compact model of nanowire junctionless gate-all-around MOSFET implemented in verilog-A for circuit simulation." *Silicon* 14 (16): 10967-10976.

Smaani, Billel, Fares Nafa, Abhishek Kumar Upadhyay, Samir Labiod, Shiromani Balmukund Rahi, Mohamed Salah Benlatreche, Hamza Akroum, Maya Lakhdara, and Ramakant Yadav. 2024. "Compact modeling of junctionless gate-all-around MOSFET for circuit simulation: Scope and challenges." In *Device Circuit Co-Design Issues in FETs*, pp. 57-78. CRC Press.

Trevisoli, Renan Doria, Rodrigo Trevisoli Doria, Michelly de Souza, Samaresh Das, Isabelle Ferain, and Marcelo Antonio Pavanello. 2012. "Surface-potential-based drain current analytical model for triple-gate junctionless nanowire transistors." *IEEE Transactions on Electron Devices* 59 (12): 3510-3518.

Tsormpatzoglou, A., D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, G. Pananakakis, and R. Clerc. 2009. "A compact drain current model of short-channel cylindrical gate-all-around MOSFETs." *Semiconductor Science and Technology* 24 (7): 075017.

Wang, Juncheng, Gang Du, Kangliang Wei, Kai Zhao, Lang Zeng, Xing Zhang, and Xiaoyan Liu. 2014. "Mixed-mode analysis of different mode silicon nanowire transistors-based inverter." *IEEE Transactions on Nanotechnology* 13 (2): 362-367.

Yu, Yun Seop. 2014. "A unified analytical current model for N-and P-type accumulation-mode (junctionless) surrounding-gate nanowire FETs." *IEEE Transactions on Electron Devices* 61 (8): 3007-3010.

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